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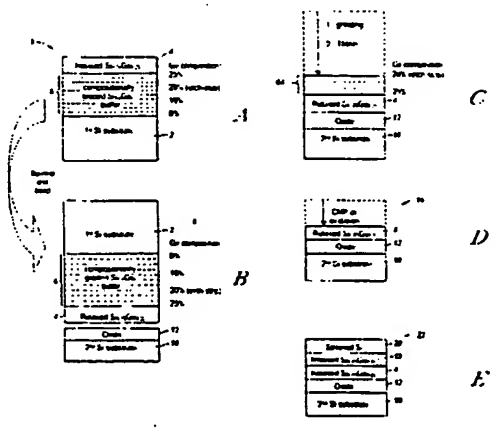
(54) Title: A METHOD FOR SEMICONDUCTOR DEVICE FABRICATION



(57) Abstract: A method of fabricating a semiconductor structure. According to one aspect of the invention, on a first semiconductor substrate, a first compositionally graded $Si_{1-x}Ge_x$ buffer is deposited where the Ge composition x is increasing from about zero to a value less than about 20%. Then a first etch-stop $Si_{1-y}Ge_y$ layer is deposited where the Ge composition y is larger than about 20% so that the layer is an effective etch-stop. A second etch-stop layer of strained Si is then grown. The deposited layer is bonded to a second substrate. After that the first substrate is removed to release said first etch-stop $Si_{1-y}Ge_y$ layer. The remaining structure is then removed in another step to release the second etch-stop layer. According to another aspect of the invention, a semiconductor structure is provided. The structure has a layer in which semiconductor devices are to be formed. The semiconductor structure includes a substrate, an insulating layer, a relaxed SiGe layer where the Ge composition is larger than approximately 15%, and a device layer selected from a group consisting of, but not limited to, strained-Si, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, Ge, GaAs, III-V materials, and II-IV materials, where Ge compositions y and z are values between 0 and 1.

WO 02/082514 A1

A METHOD FOR SEMICONDUCTOR DEVICE FABRICATION

PRIORITY INFORMATION

This application claims priority from provisional application Ser. No. 60/281,502 filed April 4, 2001.

BACKGROUND OF THE INVENTION

The invention relates to the production of a general semiconductor substrate of relaxed $Si_{1-x}Ge_x$-on-insulator (SGOI) for various electronics or optoelectronics applications, the production of strained Si or strained SiGe field effect transistor (FET) devices on SGOI, and the production of monocrystalline III-V or II-VI material-on-insulator substrates.

Relaxed SGOI is a very promising technology as it combines the benefits of two advanced technologies: the conventional SOI technology and the disruptive SiGe technology. The SOI configuration offers various advantages associated with the insulating substrate, namely reduced parasitic capacitances, improved isolation, reduced short-channel-effect, etc. The SiGe technology also has various advantages, such as mobility enhancement and integration with III-V devices.

One significant advantage of the relaxed SGOI substrate, is to fabricate high mobility strained-Si, strained-$Si_{1-x}Ge_x$ or strained-Ge FET devices. For example, strained-Si MOSFETs can be made on the SGOI substrate. The strained-Si MOSFETs on the SGOI has attracted attention because it promises very high electron and hole mobilities, which increase the speed of the electronic circuit. Other III-V optoelectronic devices can also be integrated into the SGOI substrate by matching the lattice constants of III-V materials and the relaxed $Si_{1-x}Ge_x$. For example, a GaAs layer can be grown on $Si_{1-x}Ge_x$-on-insulator where x is equal or close to 1. SGOI may serve as an ultimate platform for high speed, low power electronic and optoelectronic applications.

There are several methods for fabricating SGOI substrates and SGOI FET devices. In one method, the separation by implantation of oxygen (SIMOX) technology is used to produce SGOI. SIMOX uses a high dose oxygen implant to bury a high concentration of oxygen in a $Si_{1-x}Ge_x$ layer, which will then be converted into a buried oxide (BOX) layer upon annealing at a high temperature. One of the main drawbacks is the quality of the resulting $Si_{1-x}Ge_x$ film and the BOX layer. In addition, the Ge segregation during the high temperature anneal also limits the amount of Ge composition to a value that is low, such as 10%. Due to the low Ge composition, the device

not an ideal SGOI substrate and the silicon layer is unnecessary, and may complicate or undermine the performance of devices built on it. The relaxation of the resultant SiGe film and quality of the resulting structure are main concerns.

In a recent method, relaxed $Si_{1-x}Ge_x$-on-insulator is produced by using 20% SiGe layer as an etch-stop. First a compositionally graded $Si_{1-x}Ge_x$ buffer (where x is less than about 0.2) and then a uniform $Si_{1-y}Ge_y$ etch-stop layer (where y is larger than about 0.2) are deposited on the first substrate. Then the deposited layer is bonded to a second insulating substrate. After removing the first substrate and graded buffer layer utilizing the $Si_{1-y}Ge_y$ as an etch-stop, a $Si_{1-y}Ge_y$-on-insulator (SGOI) results. The method makes use of an experimental discovery that $Si_{1-y}Ge_y$ with Ge composition larger than about 20% is a good etch-stop for all three conventional Si etchant systems, KOH, TMAH and EDP, and the selectivity is better than the conventional p^{++} etch stop. In this method the etch-stop $Si_{1-y}Ge_y$ layer is part of the final SGOI structure. However, as the Ge composition in the final SGOI structure is fixed by the etch-stop $Si_{1-y}Ge_y$, if the desired Ge composition in the final SGOI structure is much higher or lower than 0.2, the above method is not practical. If it is much lower than 0.2, for example 0.1, $Si_{0.9}Ge_{0.1}$ is not a good etch stop at all. If it is much larger than 0.2, the Ge composition difference between the etch-stop layer and surface layer in the grade buffer is too big and there is large lattice constant difference between the two layers, which prevents the growth of a relaxed etch-stop $Si_{1-y}Ge_y$ layer with good quality.

From above, clearly an improved method is needed to fabricate a relaxed SGOI substrate with high Ge composition and wide range of Ge composition. An improved method is needed to fabricate strained-Si or strained-SiGe FET devices on SGOI substrate with high Ge composition.

SUMMARY OF THE INVENTION

According to one aspect of the invention, the invention provides a method of semiconductor device fabrication, and more specifically, a method of production of a general semiconductor substrate of relaxed SGOI for various electronics or optoelectronics applications, a method of production of strained Si or strained SiGe FET devices on SGOI, and the production of monocrystalline III-V or II-VI material-on-insulator substrates. The invention provides a method of producing a relaxed $Si_{1-x}Ge_x$-on-insulator substrate with high Ge composition and wide range of Ge composition, and the Ge composition may be much less or much higher than 20%. The invention provides an improved method to fabricate

Fig. 2. is a block diagram of a compositionally graded $Si_{1-x}Ge_x$ buffer 30. The compositionally graded $Si_{1-x}Ge_x$ buffer 30 is a multi-layer structure where the Ge composition in each layer is changing gradually from a beginning value to a final value. For example, the compositionally graded $Si_{1-x}Ge_x$ buffer 30 shown in Fig. 2 has 16 layers, and the Ge composition x in the first layer is 0% and is increasing gradually to 2%, 4%, 6% until 30% in the last layer (layer 16). Such a compositionally graded $Si_{1-x}Ge_x$ buffer 30 allows a high quality relaxed $Si_{0.7}Ge_{0.3}$ layer to be grown on the top of the buffer with low threading dislocation density.

Referring to Figs. 1(a)-1(d), a compositionally graded $Si_{1-x}Ge_x$ buffer 6 is epitaxially grown on a 4-inch Si (100) substrate 2, where the Ge composition x is increasing gradually from zero to 25% with a grading rate of 10% Ge/μm. Within the compositionally graded $Si_{1-x}Ge_x$ buffer 6, a portion of the buffer 6 with Ge composition larger than about 20% forms a natural etch stop. A 2.5 μm-thick undoped, relaxed $Si_{0.75}Ge_{0.25}$ cap layer 4 is then deposited, as shown in Fig. 1(a). The slow grading rate and high growth temperature result in a completely relaxed cap layer 4 with threading dislocation densities of $\sim 10^5$ cm^{-2}. As shown in Fig. 1(b), the wafer 2 is then flipped over and bonded to a second Si substrate 10, which is thermally oxidized. The oxide 12 in the second substrate will become the insulator layer in the final SiGe-on-insulator substrate. The bonded pair is then annealed at 850 °C for 1.5 hrs. The bonded pair is grounded to remove the donor wafer substrate 8, as shown in Fig. 1(c). The wafer 8 is then subjected to a TMAH solution to etch away a portion of the compositionally graded $Si_{1-x}Ge_x$ buffer 6 with Ge composition less than 20%. The etching process stops approximately at a 20% SiGe layer 14 within the compositionally graded $Si_{1-x}Ge_x$ buffer 6 and the 20% SiGe layer 14 is used as a natural etch stop.

After performing the etching process, the remaining portion of the compositionally graded $Si_{1-x}Ge_x$ buffer 14 with a Ge composition between 20% to 25% and part of the relaxed $Si_{0.75}Ge_{0.25}$ layer 4 are removed by chemical-mechanical polishing (CMP), resulting in a relaxed $Si_{0.75}Ge_{0.25}$-on-insulator substrate, as shown in Fig. 1(d). The CMP process is also essential in planarizing the SGOI surface for epitaxial regrowth in the next step. As shown in Fig. 1(e), in order to make a strained-Si device 22, a 100 nm p-type (doping 10^{16} cm^{-3}) relaxed $Si_{1-x}Ge_x$ layer 18 is grown at 850 °C with a Ge composition of 25%, followed by 8.5 nm-thick undoped strained-Si layer 20 grown at 650°C. Electronic devices may be fabricated on the above semiconductor structure. In particular, a large size strained-Si *n*-MOSFETs can be fabricated on the above structure and significant electron mobility enhancement is observed from the strained-Si MOSFETs.

where Q_b is the bulk depletion charge, Q_{inv} is the inversion charge, and ε_s is the dielectric constant of Si. Because of uncertainties in the strained-Si/$Si_{0.75}Ge_{0.25}$ doping, the bulk depletion charge Q_b is not computed from the usual $N_A x_{d,max}$ approximation. Instead, Q_b is extracted from

$$E_{ox}\varepsilon_{ox} = Q_{inv} + Q_b, \quad \text{Eq. 4}$$

where E_{ox} is the electric field in the gate oxide. As a result, the effective field can be approximated by

$$E_{eff} = [E_{ox}\varepsilon_{ox} - Q_{inv}/2] / \varepsilon_s. \quad \text{Eq. 5}$$

The inversion charge Q_{inv} is taken to be

$$C_{ox}(V_{GS}-V_T).E_{ox} \quad \text{Eq. 6}$$

and is assumed to be equal to V_{GS}/t_{ox}, which holds under the conditions of strong inversion and $V_{GS} >> V_{DS}$, such that the potential difference between the strongly-inverted Si surface and the S/D regions is negligibly small compared with the large potential drop across the thick gate oxide.

Fig. 4 is a graph demonstrating the measured effective electron mobility as a function of the effective vertical electric field on a strained-Si on SGOI. The graph also demonstrates the mobilities of two other controls, such as conventional bulk Si MOSFETs 34 and strained-Si MOSFETs 38 on relaxed bulk SiGe substrate, for comparison. Since all three devices have the same geometry and are processed simultaneously, possible errors due to factors such as the extraction of the ring geometry factor, and approximations in E_{eff} evaluation do not impact the relative comparison of the electron mobility characteristics. As shown in Fig. 4 , the measured mobility for the CZ Si control device 34 is close to the universal mobility curve 40. Fig. 4 also shows that the measured electron mobility enhancement for strained Si MOSFETs 36 fabricated on SGOI as compared to the mobility of co-processed bulk Si MOSFETs 38 is significant (~1.7 times). In addition, the electron mobilities are comparable for devices fabricated on SGOI 36 and bulk relaxed SiGe layers 38, thus demonstrating the superior mobility performance introduced by the strained-Si channel is retained in this SGOI structure. This enhancement factor of 1.7 is consistent with previously reported experimental and theoretical values for strained-Si *n*-MOSFETs on bulk relaxed SiGe films.

This demonstrates that the fabrication of relaxed SGOI structures and strained-Si FET devices on SGOI with high Ge composition of 25% is practical. This also demonstrates that strained-Si MOSFETs fabricated on a SGOI substrate can significantly

composition. The SiGe layer thickness uniformity is important. For example, to fabricate strained-Si MOSFET devices on a SGOI structure, the performance of the devices strongly depends on the thickness of the $Si_{0.2}Ge_{0.8}$ layer. A uniform SiGe layer is highly desired. To fabricate SGOI with Ge composition of 80% using the method described in Fig. 1, it necessitates the deposition of a relative thick compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition is increasing gradually from zero to 80%. A TMAH or KOH etch step etches away the portion of the compositionally graded $Si_{1-x}Ge_x$ buffer where Ge composition is less than 20% and stops at 20% SiGe layer within the compositionally graded $Si_{1-x}Ge_x$ buffer. The remaining portion of the compositionally graded $Si_{1-x}Ge_x$ buffer is still considerably thick, where Ge composition varies from about 20% to 80%. For example, the remaining portion of the compositionally graded $Si_{1-x}Ge_x$ buffer with Ge composition from 20% to 80% has a thickness of 6 μm if the buffer is grown with a grading rate of 10% Ge/μm.

This 6 μm thick buffer needs to be removed in order to explore the $Si_{0.2}Ge_{0.8}$ layer, for example by means of CMP. This removing step may induce significant non-uniformity. There are two possible sources of non-uniformity. First, the growth of the SiGe film itself may be not uniform across the whole substrate. For example, it is observed that the SiGe buffer can vary more than 10% in thickness if the surface of the Si substrate is placed in parallel to the direction of reactant gas flow in the CVD reactor during growth. In this orientation, one part of the substrate is in contact with higher concentration of gas than the other part since the gas concentration is decreasing along its flow pass as gas gets consumed. Therefore, the growth rate is different, resulting in differences of layer thickness. To avoid this non-uniformity, it is preferred that the surface of the Si substrate be placed normal to the direction of reactant gas flow in the reactor during the growth.

The second source comes from the removing process of the buffer layer. For example, if the buffer layer is removed by a polishing technique such as CMP, the CMP process may induce some uniformity. Although the CMP can improve the local uniformity, it may induce some global non-uniformity across the wafer. For example, the CMP process may polish the edge of the wafer faster than the center. As a result, the final SGOI structure has a non-uniform SiGe layer. Using two or more etch-stops, the system can improve the uniformity as described in the embodiment below.

Fig. 6 is block diagram of a SGOI substrate with improved SiGe layer uniformity using two etch stop layers, which is especially suitable for SGOI substrates with high Ge composition. As shown in Fig. 6, a compositionally graded $Si_{1-x}Ge_x$ buffer 56 is grown on a

bonding. However, as described above, CMP may induce global non-uniformity across the wafer. Moreover, in some cases, there may not be enough thickness for a surface to be polished. For example, if a layer is a strained Si etch-stop layer, its thickness is very small in order to keep it strained without relaxation, for example 10 nm.

Two approaches may be used to solve this issue. The first approach is before depositing the last thin material layer (e.g., the last layer is a strained Si layer), polish the SiGe buffer layer to achieve enough surface smoothness. Then grow the last strained Si etch-stop layer, which results in a smoother final surface. If the surface is smooth enough, the structure can be bonded directly. Even if polishing is still needed, it will reduce the thickness to be polished.

The second approach requires before bonding to deposit an additional insulating material layer like an oxide layer on the first structure. Afterward, polish this additional insulating layer to achieve enough surface smoothness, and then bond the polished insulating layer to a second substrate.

Fig. 8 is a block diagram of a $Si_{0.8}Ge_{0.2}$-on-insulator substrate with improved $Si_{0.8}Ge_{0.2}$ layer uniformity. As shown in Fig. 8, a compositionally graded $Si_{1-x}Ge_x$ buffer 84 is grown on a silicon substrate 82, where Ge composition x is increasing gradually from zero to about 20%. Then a $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 with selected thickness is deposited. The $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 will also contribute to the SiGe layer in the final $Si_{0.8}Ge_{0.2}$-on-insulator substrate. The thickness of the $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 is thick enough to sustain the selective etch process. This thickness is also chosen deliberately such that the resulting final $Si_{0.8}Ge_{0.2}$-on-insulator substrate has a desired $Si_{0.8}Ge_{0.2}$ layer thickness. For example, for the purpose of fabricating high mobility strained-Si MOSFET on $Si_{0.8}Ge_{0.2}$-on-insulator substrate, a final $Si_{0.8}Ge_{0.2}$ layer 86 thickness of 100 nm or less may be desired. After the deposition of $Si_{0.8}Ge_{0.2}$ etch-stop layer 86, an additional insulating layer is deposited, for example an oxide layer 88. The oxide layer 88 is polished by CMP to achieve surface smoothness required by wafer bonding. By doing this, the polishing of $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 is avoided. Without the polishing step, the $Si_{0.8}Ge_{0.2}$ etch-stop layer 86 can maintain its good uniformity. After flipping over and bonding to a second substrate, the first substrate is removed. After a selective etching process with TMAH or KOH, which removes the compositionally graded $Si_{1-x}Ge_x$ buffer and stops at the $Si_{0.8}Ge_{0.2}$ etch-stop layer 86, a final $Si_{0.8}Ge_{0.2}$-on-insulator substrate results. The structure has good SiGe layer uniformity. Polishing may be used to smooth the $Si_{0.8}Ge_{0.2}$ surface after etching without

CLAIMS

1. A method of fabricating a semiconductor structure comprising:

providing a first semiconductor substrate;

depositing a compositionally graded $Si_{1-x}Ge_x$ buffer on said first semiconductor substrate, where the Ge composition x is increasing from about 0% to a value larger than about 20%, wherein a portion of said compositionally graded $Si_{1-x}Ge_x$ buffer with Ge composition larger than about 20% forms a natural SiGe etch-stop layer;

depositing one or more material layers selected from the group consisting of, but not limited to, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, strained-Si, Ge, GaAs, III-V materials, and II-VI materials, where Ge compositions y and z are values between 0 and 1.

bonding said deposited layers to a second substrate;

removing said first substrate to explore said etch-stop SiGe layer which including the portion of said compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition is larger than approximately 20% ; and

removing said remaining portion of said compositionally graded $Si_{1-x}Ge_x$ buffer in order to release said one or more material layers.

2. The method of claim 1, wherein said second substrate has an insulating layer on the surface.

3. The method of claim 1 further comprising depositing an insulating layer before bonding.

4. The method of claim 1 further comprising polishing the surface of one of said deposited layers.

5. The method of claim 1 further comprising polishing the surface of said first substrate before bonding.

6. The method of claim 1 further comprising depositing one or more second material layers selected from the group consisting of, but not limited to, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, strained-Si, Ge, GaAs, III-V materials, and II-VI materials, where Ge compositions y and z are values between 0 and 1.

7. The method of claim 6 further comprising polishing the surface of said released

bonding said deposited layers to a second substrate;

removing said first substrate to release said uniform etch-stop $Si_{1-y}Ge_y$ layer ;

removing said uniform etch-stop $Si_{1-y}Ge_y$ layer; and

removing said second compositionally graded $Si_{1-z}Ge_z$ buffer.

12. The method of claim 11, wherein said second substrate has an insulating layer on the surface.

13. The method of claim 11 further comprising depositing an insulating layer before bonding.

14. The method of claim 11 further comprising polishing the surface of one of said deposited layers.

15. The method of claim 11 further comprising polishing the surface of said first substrate before bonding.

16. The method of claim 11 further comprising depositing one or more second material layers selected from the group consisting of, but not limited to, relaxed $Si_{1-y}Ge_y$ layer, strained $Si_{1-z}Ge_z$ layer, strained-Si, Ge, GaAs, III-V materials, and II-VI materials, where Ge compositions y and z are values between 0 and 1.

17. The method of claim 16 further comprising polishing the surface of said released of said one or more material layers before depositing said one or more second material layers.

18. The method of claims 11 further comprising fabricating a semiconductor device selected from the group consisting of, but not limited to, FET device, MOSFET device, MESFET device, solar cell device, and optoelectronic device.

19. A semiconductor etch-stop layer structure that includes a monocrystalline semiconductor substrate, said semiconductor etch-stop layer structure comprises:

a first compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition x is increasing from about zero to a value less than about 20%;

a uniform etch-stop $Si_{1-y}Ge_y$ layer of with a selected thickness where the Ge composition y larger than about 20%; and

a second compositionally graded $Si_{1-z}Ge_z$ buffer where the Ge composition x is decreasing from about 20% to a value less than 20%.

smaller value, a relaxed $Si_{1-y}Ge_y$ layer, a strained $Si_{1-z}Ge_z$ layer, where Ge composition y is a value between 0 and 1, a GaAs layer, a III-V material layer, and a II-VI material layer.

25. A method of fabricating a semiconductor structure comprising:

providing a first semiconductor substrate;

depositing a first compositionally graded $Si_{1-x}Ge_x$ buffer on said first semiconductor substrate, where the Ge composition x is increasing from about zero to a value less than about 20%;

depositing a first etch-stop $Si_{1-y}Ge_y$ layer on said first compositionally graded $Si_{1-x}Ge_x$ buffer where the Ge composition y is larger than about 20% so that the layer is an effective etch-stop;

depositing a second etch-stop layer of strained Si;

bonding said deposited layers to a second substrate;

removing said first substrate to release said first etch-stop $Si_{1-y}Ge_y$ layer ;

removing said remaining structure to release said second etch-stop layer; and

processing said released second etch-stop layer.

26. The method of claim 25 further comprising depositing one or more material layers before depositing said second etch-stop layer, and said one or more material layers are material layers selected from the group consisting of, but not limited to, a compositionally graded $Si_{1-z}Ge_z$ buffer where the Ge composition z is increasing from about 20% to a value much higher than 20%, a second compositionally graded $Si_{1-k}Ge_k$ buffer where the Ge composition k is decreasing from about 20% to a smaller value, a relaxed $Si_{1-z}Ge_z$ layer, a strained $Si_{1-o}Ge_o$ layer, where Ge composition o is a value between 0 and 1, a GaAs layer, a III-V material layer, and a II-VI material layer.

27. The method of claim 25 further comprising, before bonding, depositing one or more material layers selected from the group consisting of, but not limited to, a relaxed $Si_{1-z}Ge_z$ layer, a strained $Si_{1-z}Ge_z$ layer, where Ge composition z is a value between 0 and 1, a GaAs layer, a III-V material layer, and a II-VI material layer.

28. The process of claim 25, wherein said second substrate has an insulating layer on the surface.

29. The method of claim 25 further comprising depositing an insulating layer before bonding.

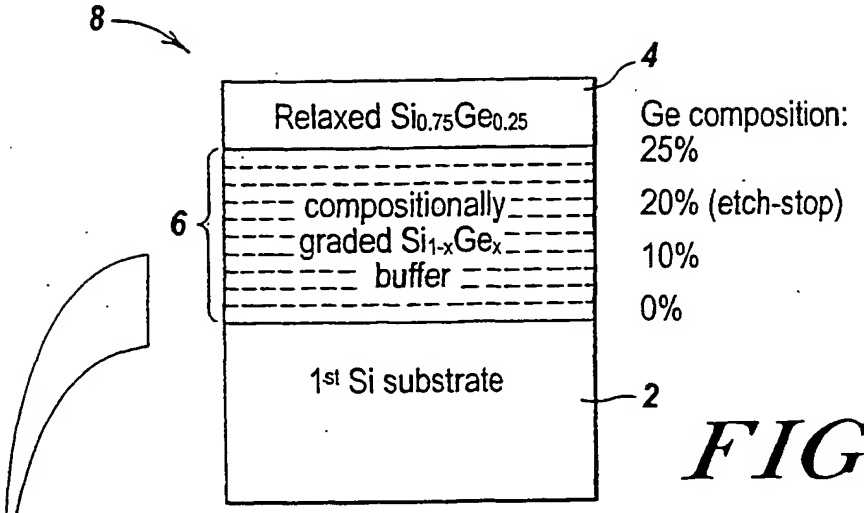

8
4
Relaxed $Si_{0.75}Ge_{0.25}$
Ge composition:
25%
6
compositionally
graded $Si_{1-x}Ge_x$
buffer
20% (etch-stop)
10%
0%
1st Si substrate
2

FIG. 1A

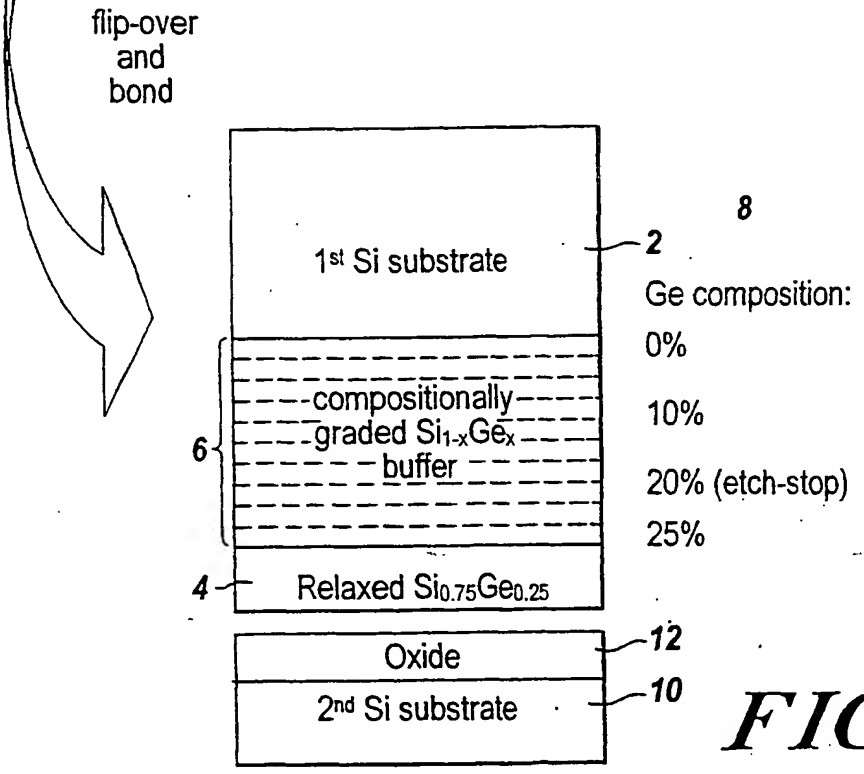

flip-over
and
bond
8
1st Si substrate
2
Ge composition:
0%
6
compositionally
graded $Si_{1-x}Ge_x$
buffer
10%
20% (etch-stop)
25%
4
Relaxed $Si_{0.75}Ge_{0.25}$
12
Oxide
10
2nd Si substrate

FIG. 1B

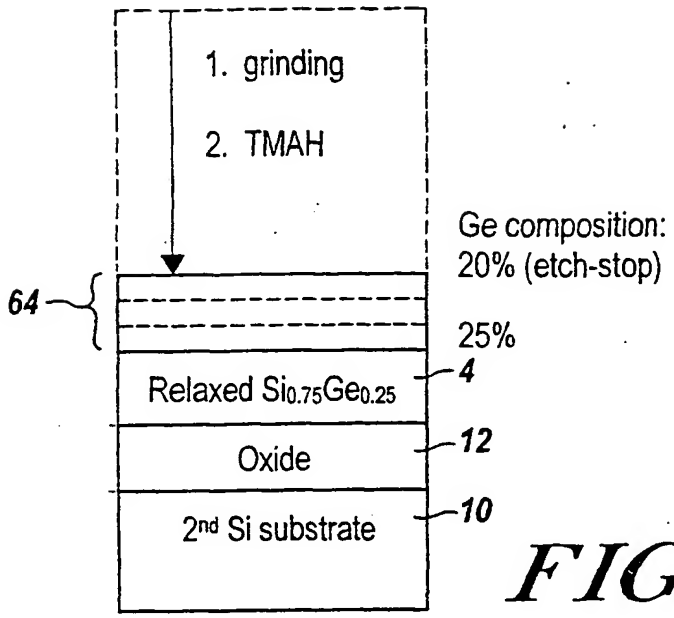


FIG. 1C

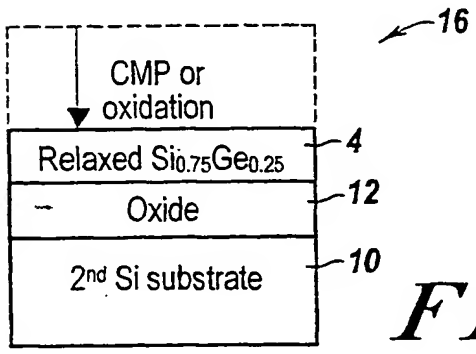


FIG. 1D

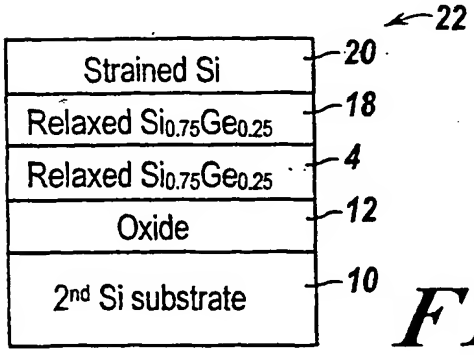


FIG. 1E

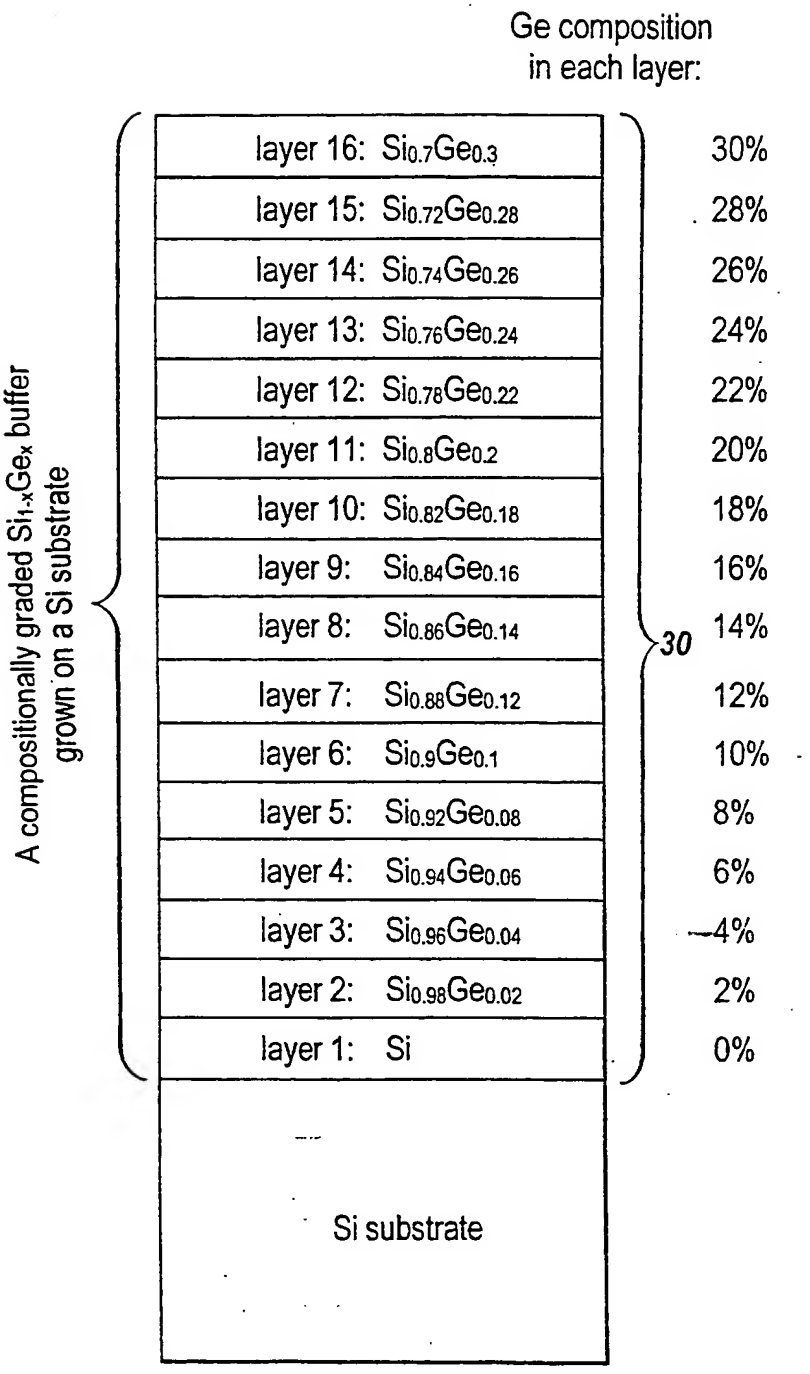

Ge composition in each layer:
A compositionally graded $Si_{1-x}Ge_x$ buffer grown on a Si substrate
layer 16: $Si_{0.7}Ge_{0.3}$ 30%
layer 15: $Si_{0.72}Ge_{0.28}$ 28%
layer 14: $Si_{0.74}Ge_{0.26}$ 26%
layer 13: $Si_{0.76}Ge_{0.24}$ 24%
layer 12: $Si_{0.78}Ge_{0.22}$ 22%
layer 11: $Si_{0.8}Ge_{0.2}$ 20%
layer 10: $Si_{0.82}Ge_{0.18}$ 18%
layer 9: $Si_{0.84}Ge_{0.16}$ 16%
layer 8: $Si_{0.86}Ge_{0.14}$ 14%
30
layer 7: $Si_{0.88}Ge_{0.12}$ 12%
layer 6: $Si_{0.9}Ge_{0.1}$ 10%
layer 5: $Si_{0.92}Ge_{0.08}$ 8%
layer 4: $Si_{0.94}Ge_{0.06}$ 6%
layer 3: $Si_{0.96}Ge_{0.04}$ 4%
layer 2: $Si_{0.98}Ge_{0.02}$ 2%
layer 1: Si 0%
Si substrate

FIG. 2

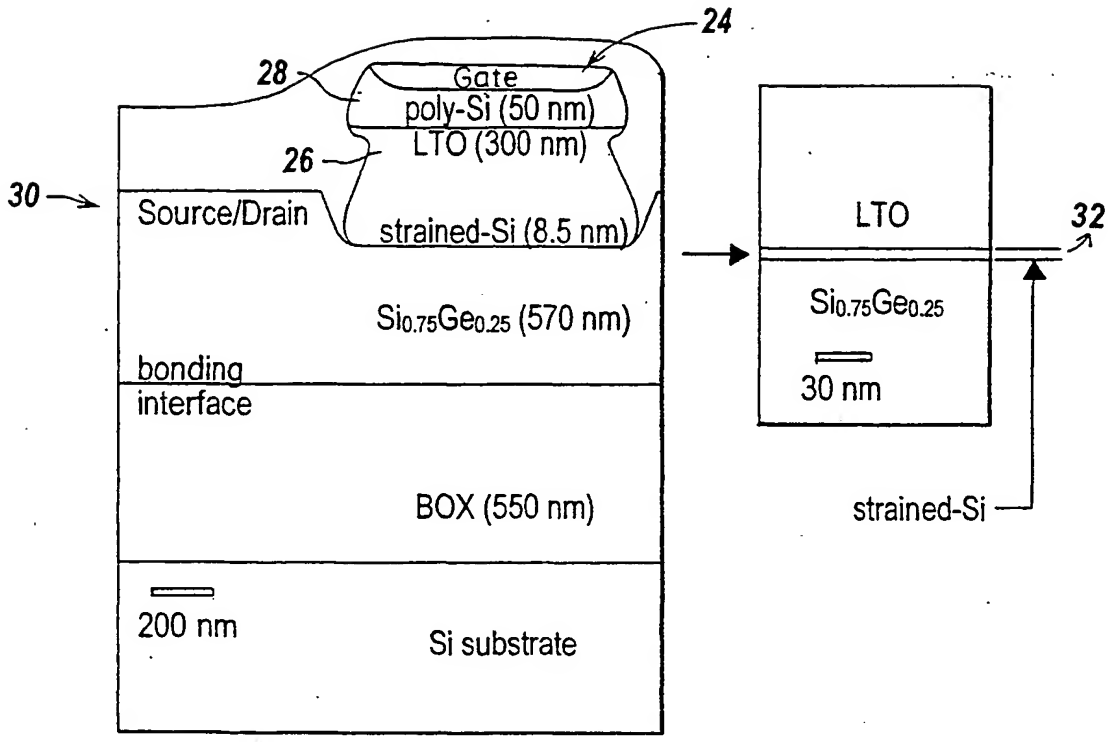

24
28
Gate
poly-Si (50 nm)
LTO (300 nm)
26
30
Source/Drain
strained-Si (8.5 nm)
Si0.75Ge0.25 (570 nm)
bonding
interface
BOX (550 nm)
200 nm
Si substrate
LTO
32
Si0.75Ge0.25
30 nm
strained-Si

FIG. 3

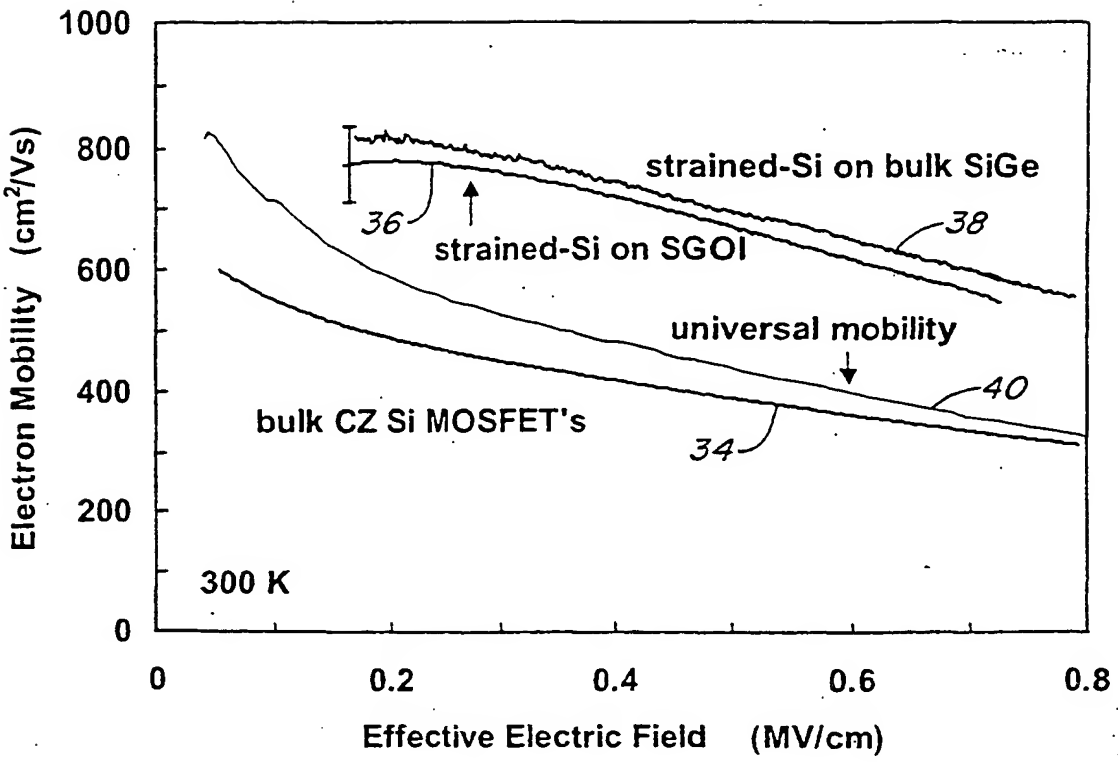

1000
800
600
400
200
0
Electron Mobility (cm²/Vs)
strained-Si on bulk SiGe
36
strained-Si on SGOI
38
universal mobility
40
bulk CZ Si MOSFET's
34
300 K
0
0.2
0.4
0.6
0.8
Effective Electric Field (MV/cm)

FIG. 4

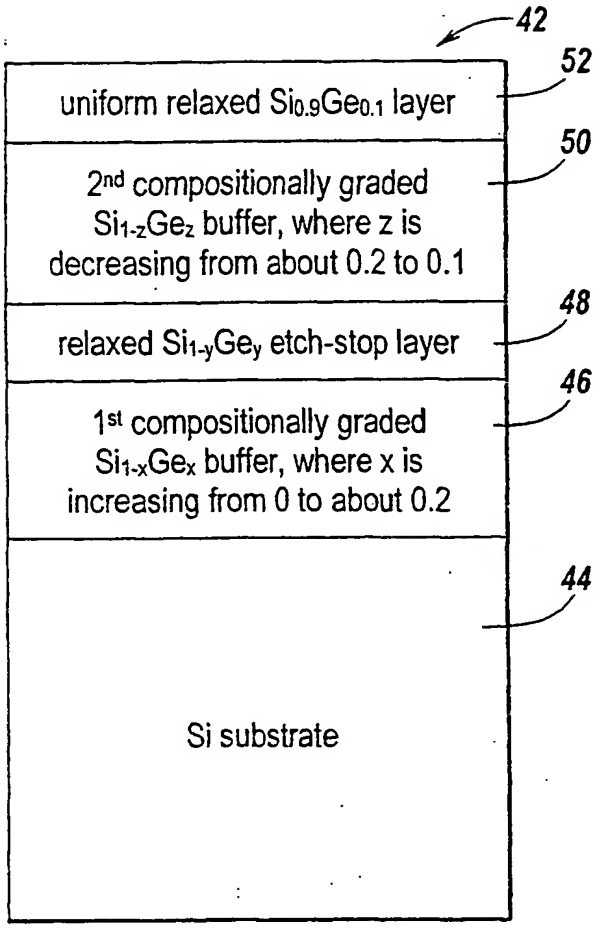

42
52
uniform relaxed $Si_{0.9}Ge_{0.1}$ layer
50
2nd compositionally graded $Si_{1-z}Ge_z$ buffer, where z is decreasing from about 0.2 to 0.1
48
relaxed $Si_{1-y}Ge_y$ etch-stop layer
46
1st compositionally graded $Si_{1-x}Ge_x$ buffer, where x is increasing from 0 to about 0.2
44
Si substrate

FIG. 5

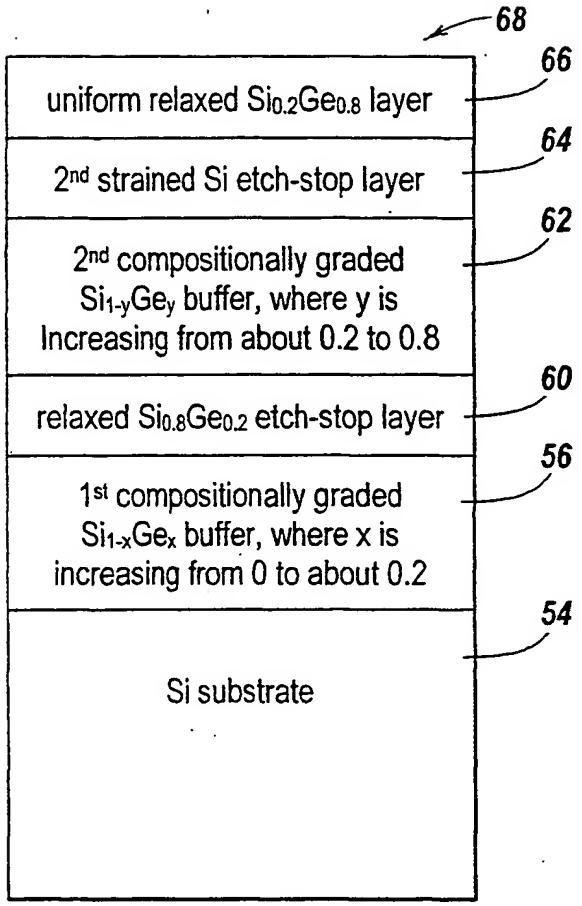

68
66
uniform relaxed $Si_{0.2}Ge_{0.8}$ layer
64
2nd strained Si etch-stop layer
62
2nd compositionally graded $Si_{1-y}Ge_y$ buffer, where y is Increasing from about 0.2 to 0.8
60
relaxed $Si_{0.8}Ge_{0.2}$ etch-stop layer
56
1st compositionally graded $Si_{1-x}Ge_x$ buffer, where x is increasing from 0 to about 0.2
54
Si substrate

FIG. 6

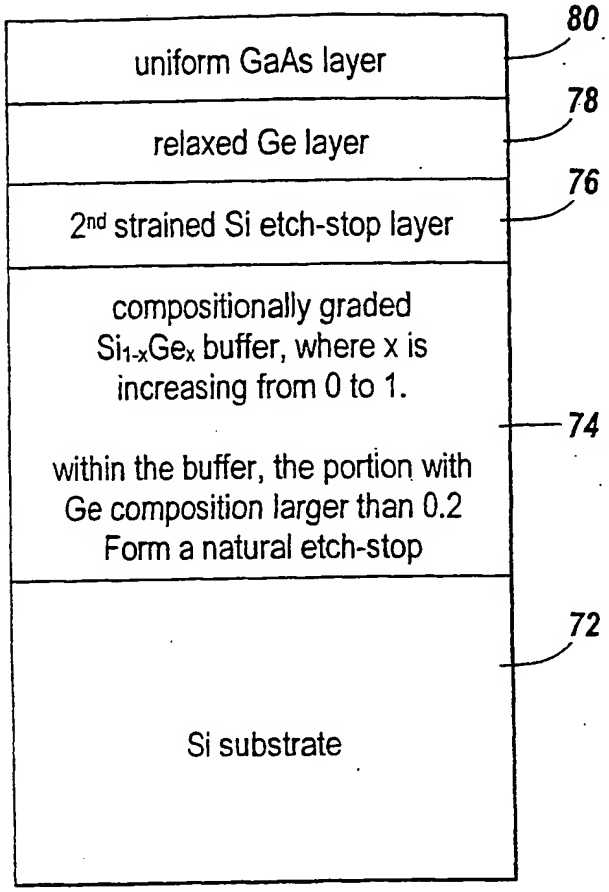

uniform GaAs layer
80
relaxed Ge layer
78
2nd strained Si etch-stop layer
76
compositionally graded Si1-xGex buffer, where x is increasing from 0 to 1.
within the buffer, the portion with Ge composition larger than 0.2 Form a natural etch-stop
74
72
Si substrate

FIG. 7

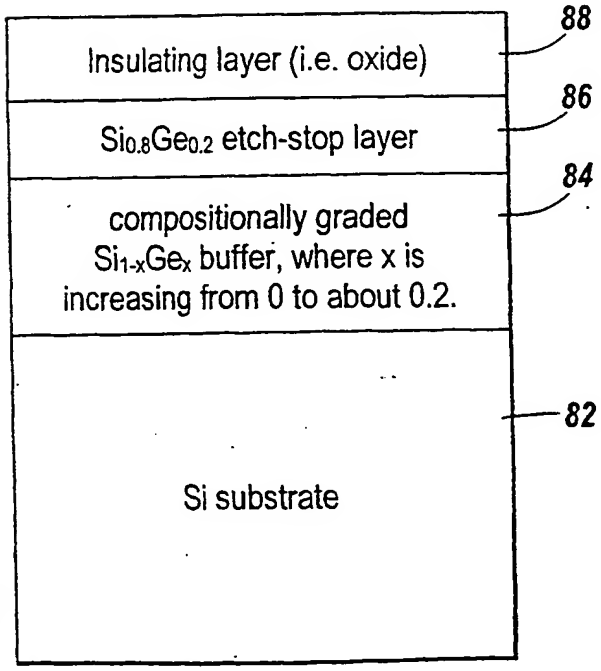

Insulating layer (i.e. oxide)
88
Si0.8Ge0.2 etch-stop layer
86
compositionally graded Si1-xGex buffer, where x is increasing from 0 to about 0.2.
84
82
Si substrate

FIG. 8

INTERNATIONAL SEARCH REPORT

ational Application No
PCT/US 02/10317

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20 H01L21/762

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 99 53539 A (MASSACHUSETTS INST TECHNOLOGY) 21 October 1999 (1999-10-21) abstract; claims; figures 1A-1D,10	1-3,6
X	US 6 059 895 A (CHU JACK OON ET AL) 9 May 2000 (2000-05-09) abstract; claims; figures	1-3,6,8, 9,11-13, 16, 18-21, 23-29, 32,34-37
Y		4,5,7, 10,14, 15,17, 30,31,33

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 September 2002	23/09/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Wirner, C

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/US 02/10317

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